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July 30, 2014

The Honorable Otis D. Wright II
U.S. District Court for the Central District of California
312 North Spring Street, Courtroom No. 11
Los Angeles, CA 90012-4701

Re: *Progressive Semiconductor Solutions LLC v. Qualcomm Technologies, Inc.*, Case No. 13-01535-ODW-JEM

The Honorable Otis D. Wright II
July 30, 2014

Dear Judge Wright:

Defendant Qualcomm Technologies, Inc. ("QTI") submits this Request for Leave to File Motion for Summary Judgment pursuant to this Court's Patent Standing Order. (Dkt 12). QTI's proposed motion is based on a single prior art reference – U.S. Patent No. 5,297,092 ("Johnson") – which anticipates all asserted claims of the patents-in-suit – U.S. Patent No. 6,473,349 (the "'349 patent") and U.S. Patent No. 6,862,208 (the "'208 patent"). An early summary judgment motion limited to one anticipating reference is appropriate here because Johnson – which predates the earlier of the two patents-in-suit by almost a decade – discloses each limitation of every asserted claim under all proposed claim constructions and no discovery, fact or expert, is necessary to resolve the motion.[1] Early summary judgment will also conserve judicial and party resources by eliminating the need for any expert discovery and most fact discovery. (*See* Scheduling and Case Management Order – Dkt 41 at 8).[2]

The Patents-in-Suit

The patents-in-suit are directed to a portion of a memory circuit, specifically an amplifier comprised of cross-coupled inverters and coupled to differential bit lines through a pair of transistors used to isolate the amplifier from the associated memory cells. The '208 patent also discloses a latch, or storage device. None of this circuitry was novel, and the patents-in-suit do not claim otherwise. The alleged point of novelty in the '349 was the use of a single signal to control both the isolation transistors and the amplifier. The alleged point of novelty in the '208 patent was the use of a latch whose timing was dependent only on the input signal.

The Johnson Reference

Johnson issued and was published on March 22, 1994, and is prior art to the patents-in-suit under 35 U.S.C. § 102(b). As discussed below, Johnson discloses an amplifier coupled to differential bit lines through a pair of pass (or isolation) transistors controlled by the sense amplifier enable signal. Johnson also discloses a pre-charge circuit and a self-timed latch.

Johnson Anticipates The Asserted Claims Of The '349 Patent

Johnson discloses each element of every asserted claim of the '349 patent. QTI is therefore entitled to judgment as a matter of law that Johnson anticipates the asserted claims of the '349 patent. Johnson anticipates claim 1 of the '349 patent as shown in the limitation-by-limitation analysis below. Johnson also anticipates claim 13 of the '349 patent, which recites elements similar to those of claim 1 in method claim form, for the same reasons as claim 1. Thus, given the low page limit, a limitation-by-limitation analysis of claim 13 is not included here.

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[1] QTI reserves all rights to file subsequent motions for summary judgment arguing that Johnson in combination, or any other reference, alone or in combination, renders the asserted claims invalid.

[2] As set forth in QTI's opposition claim construction brief (Dkt 77), QTI contends that the asserted claims of the '208 patent are invalid as indefinite. Should the Court disagree, the claims are anticipated as set forth herein.

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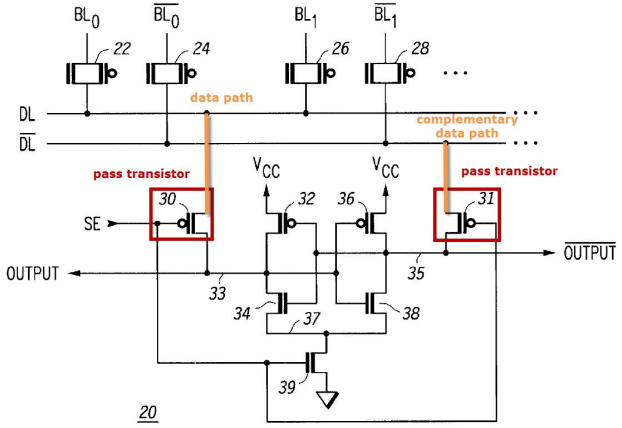
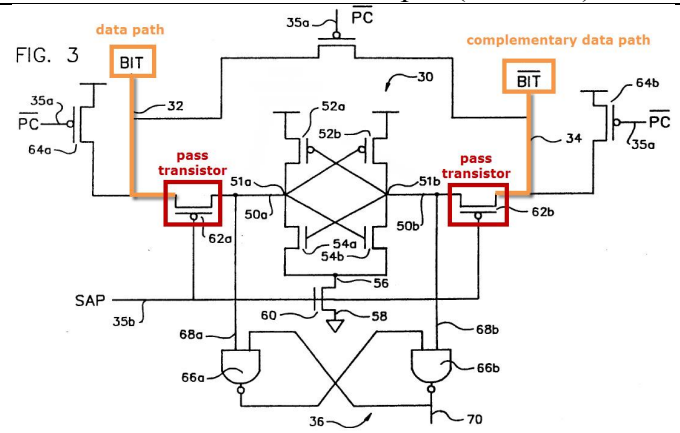
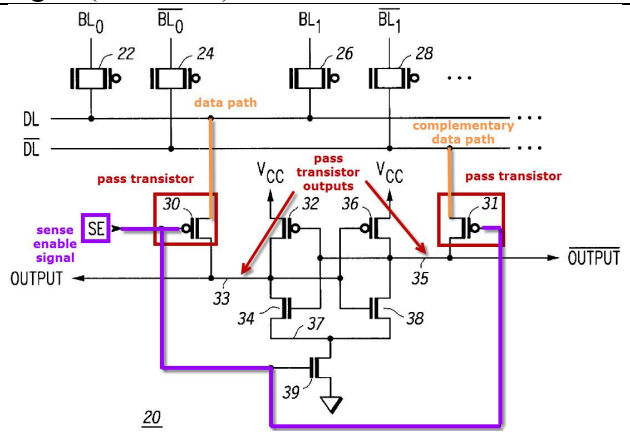
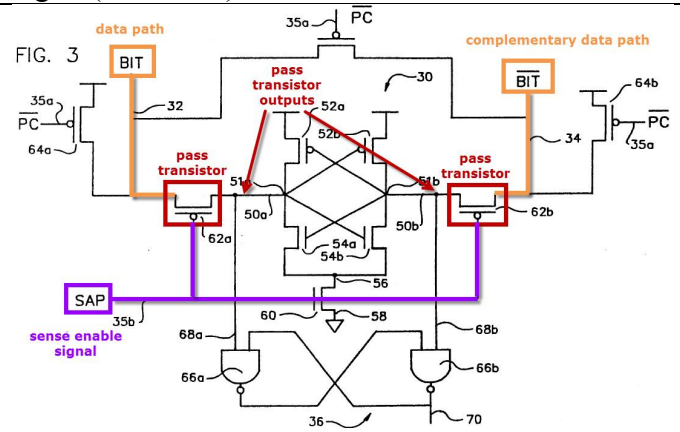
'349 patent, claim 1	**Disclosures of the '349 Patent**	**Disclosures of Johnson**
1. A sense amplifier comprising:	The '349 patent describes a "sense amp." (Abstract.)	Johnson describes a "sense amp." (Abstract.)
a pair of pass transistors having first and second inputs respectively connected to a data path and complementary data path for receiving a differential data signal,	 Fig. 2 (annotated).	 Fig. 3 (annotated).
the pair of pass transistors respectively connecting the data path and complementary data path at first and second outputs thereof in response to a sense enable signal,	 Fig. 2 (annotated).	 Fig. 3 (annotated).
the first and second inputs of the pair of pass transistors are not electrically the same as the first and second outputs thereof when the pair of pass transistors are disabled by the sense enable signal; and	Abstract: "The amplifier is operative only when the pair of pass transistors are made nonconductive."	3:45-54: "As noted above, when the SAP line 35b becomes high 76, transistors 62a and 62b become substantially non-conducting . . . Because transistors 62a and 62b are substantially non-conducting, the bit lines are not directly coupled to the sense amp 30 and latch 36 during the latching process. Because sense amp 30 is effectively cut off from the bit lines, no

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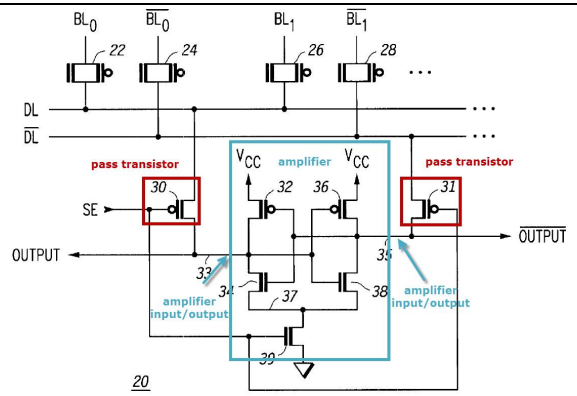
<table>
<tr><td></td><td></td><td>charging of the bit lines will occur.”</td></tr>
<tr><td>an amplifier having a first input connected to the first output of the pair of pass transistors, a second input connected to the second output of the pair of pass transistors, and first and second outputs for providing sense amplifier data signals in complementary form,</td><td> 

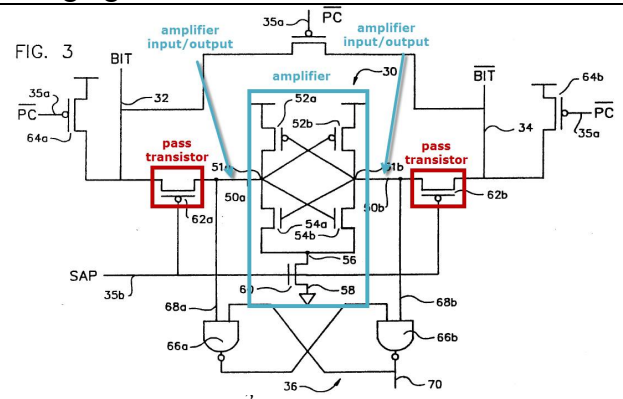
Fig. 2 (annotated).</td><td> 

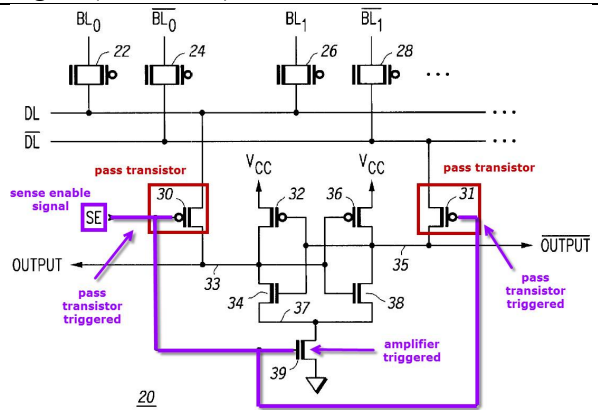
Fig. 3 (annotated).[3]</td></tr>
<tr><td>the amplifier being controlled by the sense enable signal and being operative only when the pair of pass transistors are made nonconductive by the sense enable signal.</td><td> 

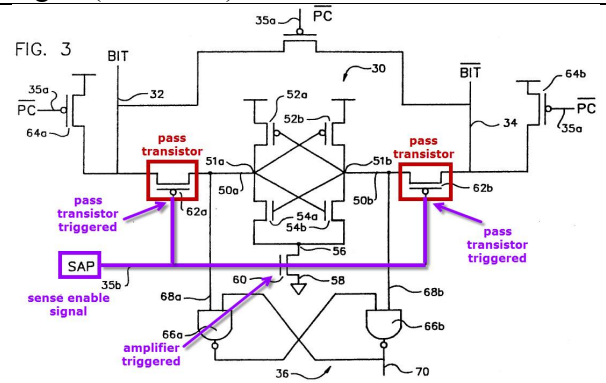
Fig. 2 (annotated).</td><td> 

Fig. 3 (annotated).</td></tr>
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Johnson Anticipates The Asserted Claims Of The ‘208 Patent

Johnson discloses each element of every asserted claim of the ‘208 patent. QTI is therefore also entitled to judgment as a matter of law that Johnson anticipates the asserted claims of the ‘208 patent. Johnson anticipates claim 1 of the ‘208 patent as set forth below.

‘208 patent, claim 1	Disclosures of the ‘208 Patent	Disclosures of Johnson
1. A memory device, comprising:	The ‘208 Patent discloses a memory device comprising a plurality of memory cells coupled to a	Johnson discloses a plurality of memory cells, each of the plurality of memory cells coupled to a bit line. (2:46-49.)

[3] The ‘349 patent confirms that an amplifier input may also serve as an output. (‘349 patent at 5:31-36)

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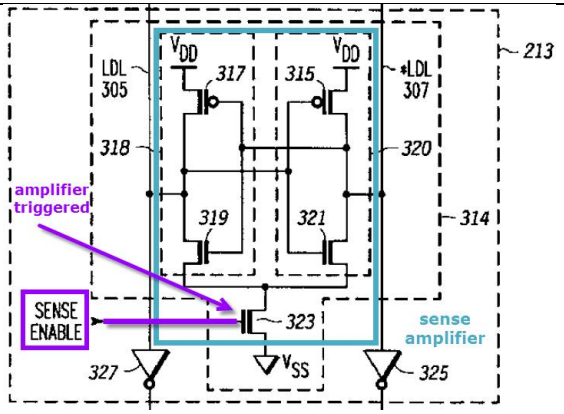
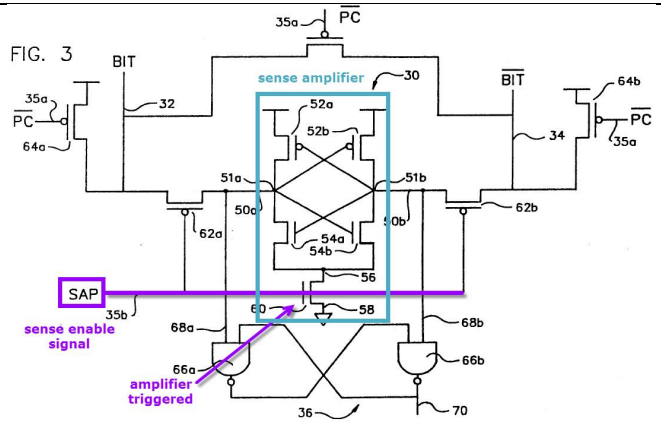
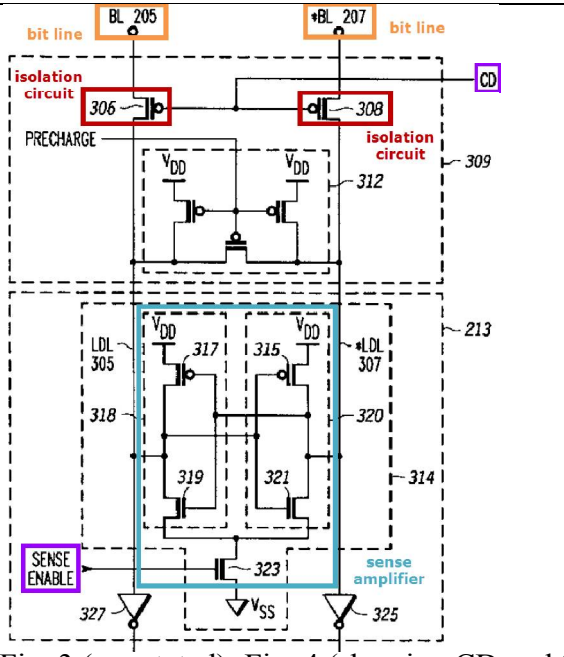
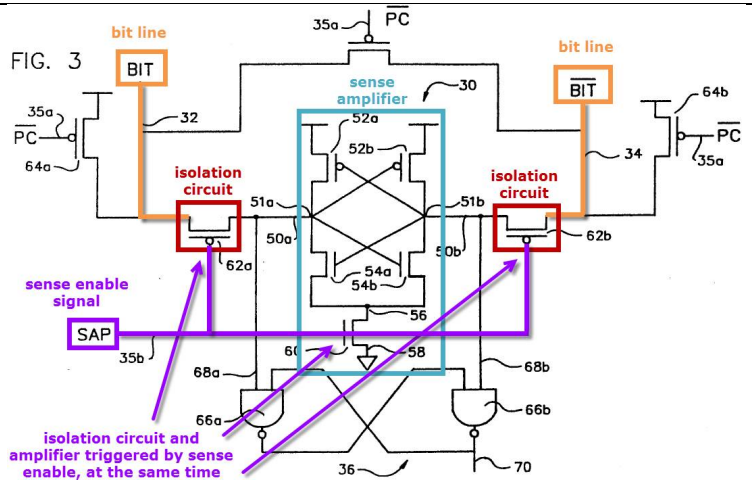
a plurality of memory cells, each of the plurality of memory cells coupled to a bit line;	bit line. (Abstract.)	
a sense amplifier for amplifying a data signal from a selected one of the plurality of memory cells via the bit line to provide an amplified data signal in response to asserting a sense enable signal;	 Fig. 3 (annotated).	 Fig. 3 (annotated).
an isolation circuit, coupled between the bit line and the sense amplifier, the isolation circuit for decoupling the selected one of the plurality of memory cells from the sense amplifier at about the same time as the assertion of the sense enable signal; and	 Fig. 3 (annotated); Fig. 4 (showing CD and SENSE ENABLE signals asserted at the same time).	 Fig. 3 (annotated). 3:45-52: "As noted above, when the SAP line 35b becomes high 76, transistors 62a and 62b become substantially non-conducting . . . Because transistors 62a and 62b are substantially non-conducting, the bit lines are not directly coupled to the sense amp 30 and latch 36 during the latching process."

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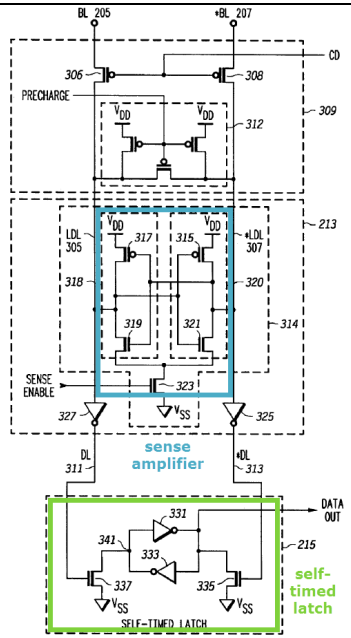
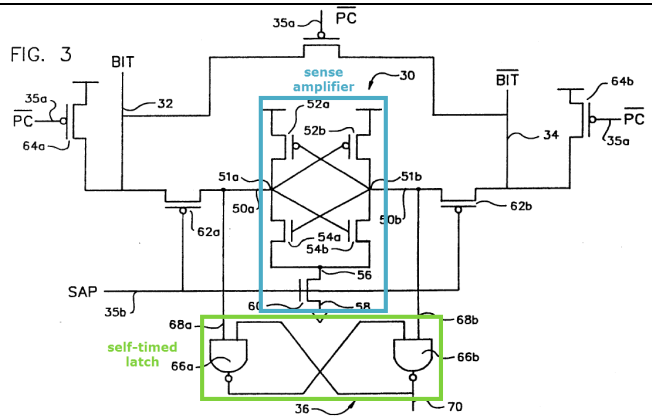
a self-timed storage device, coupled to the sense amplifier, for storing data corresponding to the amplified data signal only in response to the amplified data signal.	 Fig. 3 (annotated).	 Fig. 3 (annotated). The self-timed storage device 36 stores data corresponding to the amplified data signal received on inputs 68a and 68b, only in response to the amplified data signal received on inputs 68a and 68b. (4:33-36: "The data on the bit lines evaluated by the sense amp is automatically latched without requiring the generation of other timing signals to effect the latching.")

Johnson anticipates the asserted claims depending from claim 1, namely claims 2, 4, 7, 8, and 9. Johnson discloses that the memory device is implemented on an integrated circuit, as required by claim 2. Johnson at 1:56-2:7. Johnson discloses that the data signals and amplified data signals are differential signals, as required by claim 4. Johnson at 2:51-59. Johnson also discloses that the sense amplifier 30 comprises a pair of cross-coupled inverters (one inverter consisting of transistors 52a and 54a, the other of transistors 52b and 54b) that amplify the differential data signals to provide the amplified differential data signals in response to the sense enable signal SAP. Johnson at 3:57-59. Johnson also discloses, as required by claim 7, that the differential data signal is provided on bit lines BIT 32 and $\overline{\text{BIT}}$ 34 and that the isolation circuit comprises a first transistor 62a for selectively coupling BIT 32 to a first data line (node 51a) and a second transistor 62b for selectively coupling $\overline{\text{BIT}}$ 34 to a second data line (node 51b). Johnson at Fig. 3; 3:14-22. As required by claim 8, the sense amplifier 30 is coupled to the first and second data lines (nodes 51a and 51b), and the first second isolation transistors 62a and 62b selectively couple the first and second bit lines BIT 32 and $\overline{\text{BIT}}$ 34 to the sense amplifier 30, respectively. *Id*. Johnson also discloses the pre-charge circuit of claim 9. Johnson at 2:59-62. The pre-charge circuit of Johnson is coupled to and pre-charges the first and second data lines (nodes 51a and 51b) prior to the assertion of the sense enable signal SAP. Johnson at Figs. 4A and 4B; 3:40-42.

Johnson also anticipates claim 22 of the '208 patent, which recites elements similar to those of claim 1 in method claim form, for the same reasons as claim 1. Thus, given the low page limit, a limitation-by-limitation analysis of claim 22 is not included here. Claim 25 of the '208 patent merely adds pre-charging to claim 22, which Johnson likewise discloses. Johnson at 2:59-62.

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Respectfully Submitted,

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